

In the Specification:

Please move the statement reading:

C3 "This is a division of Patent Application Ser. No. 09/431,236,
filed on 11/1/1999, now U.S. Patent 6,297,098." ~~HE~~

to page 1, line 1 of the Specification.

In the Claims:

Please Replace Claim 29 with Rewritten Claim 29 as follows:

C1 29. (AMENDED REWRITTEN) A stacked gate memory cell pair
having a graded doubly diffused drain (DDD) profile
exhibiting minimum disturb voltage difference comprising:

5 a semiconductor substrate of a first conductivity type
having active and passive regions defined and having a top
surface;

a pair of stacked gates overlying the substrate surface,

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10 each said stacked gate having a gate oxide layer overlying
the substrate, a floating gate layer overlying the gate
oxide layer, an inter-gate oxide layer overlying the
floating gate, a control gate overlying the inter-gate
layer, sidewall spacers conforming to said stacked gates;

15 source regions of a second conductivity type formed within
said substrate and adjacent to each of said stacked gates;

a common drain region of a second conductivity type formed
20 within said substrate and defined between each pair of said
stacked gates;

channel regions within said substrate lying beneath said
stacked gates and defined between said source regions and
25 said common drain region;

a heavily doped implanted region within said common drain
region;

30 a lightly doped implanted region beneath and surrounding
said heavily doped implanted region wherein said lightly
doped and said heavily doped implanted regions are smoothly

graded doping profiles that extend from said common drain region toward the center of said channel region, wherein
35 said smoothly graded doping profiles are defined by tilt angle impurity implantation and minimal thermal diffusion, and wherein said smoothly graded doping profiles provide minimal inter-memory cell disturb voltage difference.

C1
Canceled

Please Reinstate Canceled Claim 30 with New Amendments as follows:

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30. (REINSTATED AND AMENDED) A stacked gate memory cell pair of Claim 29, wherein said lightly doped implanted region comprises phosphorous ions at a dosage level between about 1×10^{13} to 5×10^{13} atoms/cm³.

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Please Reinstate Canceled Claim 31 with New Amendments as follows:

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31. (REINSTATED AND AMENDED) A stacked gate memory cell pair of Claim 29, wherein said heavily doped implanted region comprises arsenic ions at a dosage level between about 1×10^{15} to 5×10^{15} atoms/cm³.

Please Add New Claim 32 as follows:

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32. (NEW) A stacked gate memory cell pair of Claim 29, wherein said minimal inter-memory cell disturb voltage difference is about $|0.18V|$.

~~Please Add New Claim 33 as follows:~~

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33. (NEW) A stacked gate memory cell pair of Claim 29, wherein said gate oxide layer has a thickness of between about 80 to 95 Å.

~~Please Add New Claim 34 as follows:~~

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34. (NEW) A stacked gate memory cell pair of Claim 29, wherein said floating gate has a thickness of between about 1000 to 2000 Å.

~~Please Add New Claim 35 as follows:~~

37

35. (NEW) A stacked gate memory cell pair of Claim 29, wherein said inter-gate oxide layer has a thickness of between about 120 to 160 Å.

~~Please Add New Claim 36 as follows:~~

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36. (NEW) A stacked gate memory cell pair of Claim 29,
wherein said control gate has a thickness of between about
1500 to 2000 Å.

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~~Please Add New Claim 37 as follows:~~

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37. (NEW) A stacked gate memory cell pair of Claim 29,
wherein said sidewall spacers on said stacked gate have a
thickness of between about 1200 to 1500 Å.

~~Please Add New Claim 38 as follows:~~

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38. (NEW) A stacked gate memory cell pair of Claim 29,
wherein said impurity implantation tilt angle is between
about 40 to 50 degrees from the horizontal.

REMARKS

Examiner Pizarro is thanked for the thorough examination
and search of the subject Patent Application. Claim 29 has been